REMARKS/ARGUMENTS

Claims 2-27, and 29-34 remain pending in the application with the present amendments. All of these claims stand rejected in the final Office Action dated August 5, 2003. Claims 3, 20-21, 23-24, and 32 currently stand withdrawn.

The undersigned appreciates the courtesy of the Examiner in granting the telephonic interview that was held November 5, 2003. During the interview, the features distinguishing the presently claimed invention were discussed in relation to the art cited by the Examiner. During the interview, particular attention was given to features of the claimed methods of making a multi-layer circuit assembly which distinguish them from U.S. Patent No. 6,098,282 to Frankeny et al. ("*Frankeny*"). Foremost, it was discussed the clear intent and clear description of the cited portions of *Frankeny* (FIGS. 13-22) that limit its application to capacitors. The conflicting goals of the capacitor art and those of circuit assemblies were also discussed. Further, it was also discussed the lack of teachings in *Frankeny* regarding multi-layer circuit assemblies, particularly the complete lack of teachings in *Frankeny* of multi-layer circuit assemblies having outer metal layers which are patterned to form signal lines.

Recapping the argument presented in the interview, in the art of capacitors, one seeks to maximize capacitance according to the formula: capacitance C = kA/d, k being the dielectric constant, A the area of a capacitor plate which opposes another capacitor plate, and d the distance between plates. Accordingly, in the art of capacitors, one seeks to maximize the dielectric constant and minimize the plate separation distance d. This is precisely what *Frankeny* shows by the selection of a capacitor dielectric 29 having "an extremely high dielectric constant, typically in the range of 500."(col. 6, lns. 6-7), and by the formation of a very thin (1μm or

smaller) capacitor dielectric 29 from a thin layer of sol-gel (col. 5, lns. 47-51 and col. 6, lns. 1-12).

By contrast, in the art of circuit assemblies, one seeks to avoid capacitance because it degrades the transfer of signals on a circuit assembly. Accordingly, when signal lines overlie other conductive elements such as a ground plane, power plane or other signal lines, the spacing between them is kept desirably large. In addition, the dielectric materials used in circuit assemblies tend not to have extremely high dielectric constants. Also, although signal lines often run to and from capacitors for specific purposes such as filtering or decoupling, capacitors do not incorporate signal lines.

For the foregoing reasons, *Frankeny* does not teach or suggest a multi-layer circuit assembly, does not relate to multi-layer circuit assemblies and is not properly combinable with references from the art of circuit assemblies. *Frankeny*'s teachings regarding a multi-layer capacitor structure are clearly far removed from the teachings of multi-layer circuit assemblies having outer layers patterned to form signal lines as presently claimed.

The amendments made herein further highlight the clear grounding of the claimed invention in the art of multi-layer circuit assemblies, as opposed to capacitors. By the present Amendment, claim 1 is cancelled and claim 2 is amended to incorporate all of the recitations of claim 1 from which it formerly depended. Similarly, claim 28 is cancelled and claim 29 is amended to incorporate all of the recitations of claim 28 from which it formerly depended. The remaining claims are amended to depend from either claim 2 or claim 29, respectively. As no other changes are currently being made to the claims, it is submitted that the amendments made to the now pending claims are to form only rather than to substance, and not for a reason substantially related to their patentability. Further, the

amendments should be entered because they place the application in better condition for appeal, and do not require further consideration and/or a new search.

Moreover, U.S. Patent No. 5,160,579 to Larson issued November 3, 1992 ("*Larson*") does not provide the teachings which *Frankeny* lacks relative to the claimed invention. In particular Larson does not teach or suggest:

> patterning said outer metal layers such that at least some of said metallic via liners are electrically isolated from said first and second metal layers. (claims 2 and 29)

In addition, applicant points to his arguments in the prior Amendment dated May 1, 2003 regarding the cited references to *Tsukada,* and *Cziep,* and Official Notice, as failing to be properly combinable under 35 U.S.C. §103 and/or otherwise failing to provide the teachings which Frankeny lacks with respect to the presently claimed invention. Further, for the foregoing reasons, U.s. Patent No. 5,232,548 to Ehrenberg et al., and U.S. Patent No. 6,274,820 B1 to DiStefano et al., which relate to the art of circuit boards, are also not properly combinable with *Frankeny*.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If, however, for any reason the Examiner does not believe that such action can be taken at this time, it is respectfully requested that he telephone applicant's attorney at (908) 654-5000 in order to overcome any additional objections which he might have.

If there are any additional charges in connection with this requested amendment, the Examiner is authorized to charge

Deposit Account No. 12-1095 therefor.

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Respectfully submitted,

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